REMARKS

Claims 1-14 are currently pending in the present application, with Claims 2-6, 8-10, and 13-14 being canceled, and Claims 1, 7, and 11-12 being amended. Reconsideration and reexamination of the claims, as amended, are respectfully requested.

The Examiner objected to the disclosure because of various informalities. Applicants have amended the disclosure to correct the informalities.

The Examiner objected to the drawings because of various informalities. Applicants have amended the drawings to correct the informalities.

The Examiner rejected Claims 7-14 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. This rejection is moot in view of the canceled claims. With respect to Claims 7 and 11-12, Applicants have amended the claims and respectfully submit that the amended claims are compliant with 35 U.S.C. § 112.

The Examiner rejected Claims 1-7 under 35 U.S.C. § 102(b) as being anticipated by either Landis (U.S. Patent No. 4,673,904) or Cronin et al. (U.S. Patent No. 4,776,087). This rejection is moot with respect to canceled Claims 2-6, and respectfully traversed with respect to amended Claims 1 and 7.

The present invention as claimed in Claims 1 and 7 are directed to an integrated chip having an multilayer on-chip transmission line, whereby the transmission line is shielded by metal enclosures having a cross section of a square such that the width and length of the metal shield surrounding the transmission line is substantially equal. The square cross section characteristic of the metal shielding provides the transmission line with characteristic impedance greater than, for instance, a metal shielding with irregular or rectangular cross section, thereby reducing the power dissipation of the transmission line and provides a closer correlation to a off-chip coaxial cable or transmission line.

Neither Landis nor Cronin contain any disclosure or suggestion of a chip having an on-chip multilayer transmission line shielded by metal shielding having a substantially square cross

section. Rather, Landis is simply directed to a support board that includes conductor strips for connecting electronic components or devices that are affixed to the surface of the board (See, e.g., Col. 2, lines 37-47). Landis does not make any mention or suggestion of an on-chip transmission line or a transmission line embedded within a chip.

Similarly, Cronin does not contain any suggestion or teaching of an integrated chip having an on-chip transmission line whereby the transmission line is surrounded by metal shielding having a square-like cross section. Specifically, Cronin does not teach or suggest a chip having an on-chip transmission line whereby "the distance between the top and bottom conductive planes are substantially equal to the distance between the two laterally spaced terminal conductive strips," as recited in amended Claim 1. Instead, as shown in Figs. 8-11, Cronin only illustrates a coaxial wiring structure having a metal surrounding of rectangular cross section. Cronin does not contain any disclosure of an integrated chip having an on-chip transmission line that is protected by metal shielding of a square cross section, which, as discussed above, provides characteristic impedance and power dissipation properties superior to that of a metal shielding with a rectangular cross section. Accordingly, Applicants respectfully submit that amended Claims 1 and 7 are not anticipated by, nor obvious in view of, either Landis or Cronin.

The Examiner rejected Claims 11 and 13 under 35 U.S.C. § 102(b) as being anticipated by Landis. This rejection is moot with respect to canceled Claim 13 and respectfully traversed with respect to amended Claim 11. As discussed above, Landis does not contain any disclosure of an integrated chip or a chip having an on-chip transmission line. Rather, Landis is simply directed to a board having wiring structures for connecting electronic components or devices. Furthermore, Landis does not contain any disclosure of a chip having a plurality of on-chip transmission line, each of which protected by metal shielding of square-like cross section. Accordingly, Applicants respectfully submit that Claim 11 is not anticipated by, nor obvious in view of, Landis.

The Examiner rejected Claims 8-10 under 35 U.S.C. § 103(a) as being unpatentable over either Landis or Cronin in view of Young (U.S. Patent No. 5,408,053). This rejection is moot in view of the canceled claims.

In view of the foregoing, Applicants respectfully submit that all of the pending claims, as amended, are in condition for allowance. Reconsideration and reexamination of the claims are respectfully requested, and an early allowance is solicited. If the Examiner believe it would further advance the prosecution of the present application, he is respectfully requested to contact the undersigned attorney.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**".

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, Applicant petitions for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 535352000500.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The specification was amended in the following manner:

On Page 3, the heading on line 15 was amended as follows:

DETAILED DESCRIPTION OF THE INVENTION

On Page 3, the Paragraph starting at line 25 and ending at line 28 was amended as follows:

Figs. 1 and 2 depict elevational section views of the prior art strip line 1 and microstrip monolithic 5 constructions respectively. Both of these constructions are well known in the planar fabrication and microcircuit technology. In Fig. 1, the strip line comprises a metal conductor etched on top of an insulator.

On Page 3, the Paragraph starting at line 30 and ending at Page 4, line 2, was amended as follows:

The microstrip construction 5 shown in Fig. 2 comprises a pair of metal conductors 6 and 8 in spaced apart positions with one of the conductors 9 embedded within the insulation material 7. In both of these constructions, the only way to achieve field isolation is to space adjacent conductors apart. However, this uses an undesirable amount of surface area on the substrate to achieve such isolation.

On Page 4, the Paragraph starting at line 4 and ending at line 17 was amended as follows:

Referring to Fig. 3, an on-chip three layer metal-shielded monolithic transmission line of the present invention comprises, in a simple embodiment, three parallel planar thin film, conductive layers 10 which are typically one micron thick condensates of Cu, Al, or Au placed by, for example, a physical vapor deposition process such as evaporation or sputtering. Each adjacent pair of the conductive layers 10 is separated by one of a plurality of planar thin film nonconductive separator layers 20, typically an oxide deposited or grown, to form a stack 30 of alternating conductive 10 and nonconductive 20 layers. An initial one 12 and a final one 14 [ones] of said conductive layers 10 form a top and a bottom conductive planes, the conductive planes establishing a mutually registered selected width 32 of the stack 30. A center one 16 of the conductive layers 10 comprises three laterally spaced apart conductive strips 16', 16" and 16'" separated laterally by a pair of non conductive spacer layers 40, the two laterally terminal 16' and 16'" of the three conductive strips 16', 16" and 16'" being spaced at approximately the selected width 32.

On Page 4, the paragraph starting at line 31 and ending at Page 5, line 11 was amended as follows:

Referring to Fig. 4, the above-described configuration may be further extended to include additional layers such as the 5 metal layer embodiment shown. In this further embodiment, the plurality of parallel planar thin film, conductive layers 10 are formed wherein each adjacent pair of the conductive layers is separated by one of the plurality of planar thin film nonconductive separator layers 20 to form the stack of alternating conductive and nonconductive said layers 30. The initial one 12 and final one 14 [ones] of [said] conductive layers 10 form the top and bottom conductive planes as before, the conductive planes establishing the mutually registered selected width 32 of the stack. One of the conductive layers 16 between the top and the bottom conductive planes 12, 14, comprises three laterally spaced apart conductive strips 16', 16", 16'" separated by a pair of nonconductive laterally spaced apart spacer layers 40, the two laterally terminal 16', 16" of the three conductive strips being spaced approximately at the selected width 32 as in the previous embodiment.

On Page 6, the paragraph starting at line 31 and ending at Page 7, line 4 was amended as follows:

As shown in [the plain view of] Fig. 6, because the vias 22 are generally only able to be fabricated with limited lengths "L", the spaces 24 between adjacent vias 22 of one shield side wall are staggered with respect to the spaces 24 between adjacent vias 22 of the adjacent next side wall so as to provide full isolation between adjacent center conductors 16' and 16" as, for instance, when the constructions defined above are positioned side-by-side on the substrate.

On Page 7, the paragraph starting at line 13 and ending at line 16 was amended as follows:

The process further comprises the step of extending, by simple metal deposition, the initial one 12 and the final one 14 [ones] of [said] the conductive layers, as the top and the bottom conductive planes, to define the mutually registered selected width 32 of the stack 30.

In the Claims:

Claims 1, 7, and 11-12 have been amended in the following manner:

1. (Amended) [An] A chip having an on-chip multi-layer metal-shielded monolithic transmission line comprising:

[plural] a plurality of parallel planar thin film[,] conductive layers; and

[plural] a plurality of planar thin film nonconductive separator layers disposed such that each adjacent pair of the conductive layers is separated by at least one of said plurality of planar thin film nonconductive layers to form a stack of alternating conductive and nonconductive layers,

wherein an initial one and a final one of said conductive layers form a top conductive plane and a bottom conductive plane,

wherein a center one of the conductive layers comprises three laterally spaced apart conductive strips, said conductive strips separated by nonconductive material such that two laterally spaced terminal strips of the three conductive strips are spaced at a selected width from the center conductive strip,

wherein each of the nonconductive separator layers include a plurality of vias between the two laterally spaced terminal conductive strips of the three conductive strips and the top and bottom conductive planes, said plurality of vias filled with conductive material, and

wherein the distance between the top and bottom conductive planes is substantially equal to the distance between the two laterally spaced terminal conductive strips.

7. (Amended) The invention of Claim [6] 1, wherein the center conductive [strips] strip provides [a] an electrical signal carrying path.

11. (Amended) A chip having a plurality of on-chip multi-layer metal-shielded monolithic transmission lines comprising:

a plurality of parallel planar thin film[,] conductive layers, each adjacent pair of the conductive layers separated by at least one of a plurality of planar thin film nonconductive separator layers to form a stack of alternating conductive and nonconductive said layers[;],

wherein an initial one and a final [ones] one of said conductive layers forming a top conductive plane and a bottom conductive [planes] plane, [the conductive planes establishing a mutually registered selected width of the stack;]

wherein one of the conductive layers between the top and the bottom conductive planes [comprising] includes a plurality of N laterally spaced apart conductive strips, where N is an odd integer,

wherein each laterally adjacent pair of the conductive strips are separated at a predetermined width by [a] nonconductive material, [spacer layer forming N-l/2 signal carrying ones of the conductive strips, the two laterally terminal of the plurality of conductive strips being spaced at the selected width;

each of the other of the conductive layers between the one of the conductive layers and the top one of the conductive planes, and between the one of the conductive layers and the bottom one of the conductive planes, comprising a plurality of [(N-l)/2]+ 1 laterally spaced apart conductive strips, each laterally adjacent pair of the conductive strips separated by a nonconductive spacer layer, the two laterally terminal of the plurality of conductive strips being spaced at the selected width; and]

wherein the plurality of nonconductive separator layers [providing] include a plurality of metal filled vias positioned for electrically interconnecting [a plurality of the conductive strips so

as to electrically isolate each of (N-l)/2 of the signal carrying conductive strips] every other one of the laterally spaced apart conductive strips to the top and bottom conductive planes, and

wherein the distance between top conductive plane and bottom conductive plane is substantially equal to the distance between every other laterally spaced conductive strips .

12. (Amended) The transmission lines of Claim 11, wherein the plurality of vias of one of the transmission lines are staggered relative to the plurality of vias of an adjacent one of the transmission lines so as to preclude an electromagnetic line of sight path between the signal carrying conductive strips of the transmission lines.